IN THE CLAIMS:

Rewrite the claims as follows:

1. (Cancelled)

2. (Previously presented) A memory system, comprising:

a memory device; and

a controller coupled to the memory device using a data bus, the controller including:

an interface for receiving pipelined read and write commands;

a buffer that temporarily stores write data corresponding to a first address in the memory device; and

buffer control logic to transfer the write data, corresponding to the first address, from the buffer to the memory device in accordance with a current command;

wherein when the current command is a read command having an associated address that is the same as the first address, the controller delays issuance of the read command to the memory device.

3. (Previously presented) The memory system of claim 2, wherein the interface is also for receiving commands other than read and write commands.

4. (Previously presented) The memory system of claim 2, wherein the write data is transferred from the buffer to the memory device in further accordance with a previous command received by the controller.

5. (Previously presented) The memory system of claim 2, wherein the write data is transferred from the buffer to the memory device if the controller is idle during a time period.

6. (Previously presented) The memory system of claim 2, wherein the buffer comprises a first in, first out (FIFO) buffer.

7. (Previously presented) The memory system of claim 2, wherein the buffer control logic comprises a finite state machine.

8. (Previously presented) The memory system of claim 7, wherein the finite state machine is implemented in a look-up table.

9. (Previously presented) A memory system, comprising:

a memory device;

a data bus; and

a controller coupled to the memory device using the data bus, the controller including:

an interface for receiving read, write and other commands;

a buffer that temporarily stores write data corresponding to a first address in the memory device; and

buffer control logic, comprising a finite state machine, for transferring the write data corresponding to the first address from the buffer to the memory device in accordance with a current command;

wherein the controller is configured to perform a predefined operation on the read command when the current command is a read command having an associated address that is the same as the first address; and

wherein the finite state machine has at least four states, a first state corresponding to an initial idle mode of operation, a second state corresponding to a write-once-to-the-buffer mode of operation, a third state corresponding to a wait mode of operation and a fourth state corresponding to a write-twice-to-the-buffer mode of operation.

10. (Previously presented) The memory system of claim 9, wherein the finite state machine is configured to remain in the first state until a first write command is received by the controller, and the finite state machine is configured to transition to the second state when the first write command is received in a first time period and the controller stores the write data corresponding to the first write command in the buffer.

11. (Previously presented) The memory system of claim 10, wherein the finite state machine is configured to transition from the second state to the fourth state when a second write command is received in a second time period and the controller stores the write data corresponding to the second write command in the buffer.

12. (Previously presented) The memory system of claim 11, wherein the finite state machine is configured to remain in the fourth state when a third write command is received in a third time period and the controller transfers the write data corresponding to the first write command from the buffer to the memory device.

13. (Previously presented) The memory system of claim 11, wherein the finite state machine is configured to transition from the fourth state to the third state when a non-read/write command is received in a third time period and the controller transfers the write data corresponding to the first write command from the buffer to the memory device.

14. (Previously presented) The memory system of claim 13, wherein the finite state machine is configured to transition from the third state to the second state when a third write command is received in a fourth time period, the controller stores the write data corresponding to the third write command in the buffer and the controller transfers the write data corresponding to the second write command from the buffer to the memory device.

15. (Previously presented) The memory system of claim 13, wherein the finite state machine is configured to transition from the third state to the first state when a non-read/write command is received in a fourth time period and the controller transfers the write data corresponding to the second write command from the buffer to the memory device.

16. (Previously presented) The memory system of claim 13, wherein the finite state machine is configured to transition from the third state to the first state when a read command is received in a fourth time period, the controller transfers the write data corresponding to the second write command from the buffer to the memory device and the controller delays the read command if an address corresponding to the read command matches one of the addresses corresponding to the write data in the buffer.

17. (Previously presented) The memory system of claim 11, wherein the finite state machine is configured to transition from the fourth state to the third state when a read command is received in a third time period, the controller transfers the write data corresponding to the first write command from the buffer to the memory device and the controller delays the read command if an address corresponding to the read command matches one of the addresses corresponding to the write data in the buffer.

18. (Previously presented) The memory system of claim 17, wherein the finite state machine is configured to transition from the third state to the second state when a third write command is received in a fourth time period, the controller stores the write data corresponding to the third write command in the buffer and the controller transfers the write data corresponding to the second write command from the buffer to the memory device.

19. (Previously presented) The memory system of claim 17, wherein the finite state machine is configured to transition from the third state to the first state when a non-read/write command is received in a fourth time period and the controller transfers the write data corresponding to the second write command from the buffer to the memory device.

20. (Previously presented) The memory system of claim 17, wherein the finite state machine is configured to transition from the third state to the first state when a read command is received in a fourth time period, the controller transfers the write data corresponding to the second write command from the buffer to the memory device and the controller delays the read command if an address corresponding to the read command matches one of the addresses corresponding to the write data in the buffer.

21. (Previously presented) The memory system of claim 10, wherein the finite state machine is configured to transition from the second state to the third state if a command other than a second write command is received in a third time period.

22. (Previously presented) The memory system of claim 21, wherein the finite state machine is configured to transition from the third state to the second state when the second write command is received in a fourth time period, the controller stores the write data corresponding to the second write command in the buffer and the controller transfers the write data corresponding to the first write command from the buffer to the memory device.

23. (Previously presented) The memory system of claim 21, wherein the finite state machine is configured to transition from the third state to the first state when a non-read/write command is received in a fourth time period and the controller transfers the write data corresponding to the first write command from the buffer to the memory device.

24. (Previously presented) The memory system of claim 21, wherein the finite state machine is configured to transition from the third state to the first state when a read command is received in a fourth time period, the controller transfers the write data corresponding to the first write command from the buffer to the memory device and the controller delays the read command if an address corresponding to the read command matches one of the addresses corresponding to the write data in the buffer.

25. (Currently amended) A memory system, comprising:

a memory means;

a communication means; and

a controller means coupled to the memory means using the communication means, wherein the controller means receives pipelined read, write and other commands, temporarily stores write data corresponding to a first address in the memory means, transfers the write data to the memory means in accordance with a current command, and when the current command is a read ~~commend~~ command having an associated address that is the same as the first address, delays issuance of the read command.